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Attorney's Docket No. S1022.80544US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Peter BALLAM
Serial No.: 09/692,297 Patent No. 6,847,926 B1
Filing Date: October 19, 2000 Issued: January 25, 2005
For: METHOD OF DISTINGUISHING BIDIRECTIONAL PINS

Examiner: Crystal J. Barnes
Art Unit: 2121 Conf. No.: 4272

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: Examiner's Amend; Pages 3 and 4 of 7/7/04 Amend and Cols 18 and 20 of U.S. 6,847,926.
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop , Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 28, 2005.

Respectfully submitted,

Peter Ballam, Applicant

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Sir/Madam:

Patentee respectfully requests the correction of errors found in the above-captioned patent. Specifically, there is a typographical error and errors of omission in issued U.S. Patent No. 6,816,821.

In column 18, line 63 through column 19, line 6 claim 1 currently read as shown below:

> 1. A method of distinguishing between an input and output signal on a bi-directional pin of a model of a hardware **circuit the** steps of:
>
> for a bi-directional pin of **said signals** to said bi-directional pin at a reduced drive strength such that a driven signal on said bi-directional pin will be superimposed over the applied signal; and
>
> measuring the drive strength of the signal on the bi-directional pin and responsive to said measurement determining whether the bi-directional pin is an input or output. (Emphasis added)

However, this claim was amended in the amendment filed on July 7, 2004 and again by Examiner's amendment attached to the Notice of Allowance. Claim 1, as allowed should read as shown below:

> 1. A method of distinguishing between an input and output signal on a bi-directional pin of a model of a hardware **circuit, comprising the** steps of:
>
> for a bi-directional pin of **said bi-directional signals** to said bi-directional pin at a reduced drive strength such that a driven signal on said bi-directional pin will be superimposed over the applied signal; and

measuring the drive strength of the signal on the bi-directional pin and responsive to said measurement determining whether the bi-directional pin is an input or output. (Emphasis added)

In column 20, lines 4-14, claim 8 currently read as shown below:

8. A system for distinguishing between an input and output signal on a bi-directional pin of a model of a hardware circuit, said system comprising:
means for applying signals to a bi-directional pin of said model at a reduced drive strength such that a driven signal on **said pin** will be super imposed over the applied signal; and
means for measuring the drive strength of the signal on the bi-directional pin and responsive to said measurement determining whether the bi-directional pin is an input or output. (Emphasis added)

However, this claim was amended in an amendment filed on July 7, 2004 and again by Examiner's amendment attached to the Notice of Allowance. Claim 8 as allowed should read as shown below:

8. A system for distinguishing between an input and output signal on a bi-directional pin of a model of a hardware circuit, said system comprising:
means for applying signals to a bi-directional pin of said model at a reduced drive strength such that a driven signal on **said bi-directional pin** will be super imposed over the applied signal; and
means for measuring the drive strength of the signal on the bi-directional pin and responsive to said measurement determining whether the bi-directional pin is an input or output. (Emphasis added)

No such amendments were made by either the Examiner or by Patentee deleting the omitted text. In support of this Request Patentee submits herewith a highlighted copy of pages 3 and 4 of the amendment filed on July 7, 2004 and columns 18, 19 and 20 of U.S. 6,847,926.

Patentee requests that a Certificate of Correction be granted in U.S. Letters Patent No. 6,847,926 as specified herein and on the attached Certificate of Correction form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the corrections be made and that a Certificate of Correction be issued.

Patentee respectfully submits that, since the error for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a

fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop , Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 28, 2005.

Respectfully submitted,

Peter Ballam, Applicant

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XNDD

W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_2_netlist.vhd'
W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_2_cfg.vhd'
W2TB-I-SYSCMD, Running system command 'vhdlsim -nc -i w2tb_all_cct_2.control'
W2TB-I-ASSERT, no assertions detected in last simulation.
SECTION 6—general operation -only WIF (step S6)
W2TB-I-SYSCMD, Running system command 'wif_print ALL_CCT_TEST_BENCH.ow>w2tb'
SECTION 7—read into memory the second WIF file, the outputs only. This is the second database. (step S7)
W2TB-I-WIFIN, Parsing results wif file
WP-I-PINS, Encountered 7 pins in object block
WP-I-OIN, Read in object block
WP-W-PROGRESS, Percentage of vectors parsed=100%-completed
WP-I-VECS, Total of 46 vectors read
WP-I-DELTA, Smallest delta =5000.00 ps
WP-I-PIN, Read in the test patterns
SECTION 8—merge the outputs from the second WIF file into the first database. (step S8)
W2TN-S-IN, Successfully loaded results database
SECTION 9—expand the X vectors (steps S9, S10 and S11)
W2TB-I-XS, Exhaustively expanded level X states, now have 119 vectors
SECTION 10—write the second HDL test bench. (step S12)
WT2B-I-VHDL, Writing VHDL to file prefixed 'w2tb_all_cct_16'
W2TB-I-ASSERT, Adding output testing code
SECTION 11—the second HDL simulation (steps S13 and S14)
W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16_.vhd'
W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16_behav.vhd'
W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16.netlist'
W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16_cfg.vhd'
W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16.control'
SECTION 12—this checks if the X modelling is correct. If it is, no assertions will be detected. (step S14)
W2TB-I-ASSERT, no assertions detected in last simulation.
W2TB-I-SYSCMD, Running system command 'wif_print ALL_CCT_TEST_BENCH.ow>w2tb'
SECTION 13 Data prepared for SPICE (step S15)
W2TB-I-ZS, Expanded output Z states, now have 204 vectors
SECTION 14—write SPICE test bench (step S16)
W2TB-I-RES, A total of 6 resistors written to the ELDO test bench
W2TB-I-SW, A total of 72 switches written to ELDO test bench
W2TB-I-VOLT, A total of 76 voltage sources written to ELDO test bench
W2TB-I-CURRENT, a total of 0 current sources written to ELDO test bench
W2TB-S-END, ELDO test bench written
SECTION 15—run SPICE simulation (step S17)
W2TB-I-SYSCMD, Running system command '$eldodir/com/eldo-stveer w2tb_all_cct
W2TB-I-LOG the log of the eldo simulation has the following lines in it
**** 0 errors
**** 0 errors
**** 0 warnings
**** 0 warnings
SECTION 16—convert SPICE to WIF file, outputs only (step S17)
W2TB-I-SYSCMD, running system command '$WIF2TB_ROOT/bin/chi2halfwif w2tb_all_
C2W-I-START, Converting ELDO chi file 'w2rb_all_cct_32.chi' into WIF file 'w2
C2W-I-SIGNALS, Found 7 signal to convert
C2W-I-DONE, converted 269 vectors
SECTION 17—read in WIF file, reuse second database in memory (step S18)
W2TB-I-WIFIN, Parsing ELDO results wif file
WP-I-PINS, Encountered 7 pins in object block
WP-I-OIN, Read in object block
WP-W-PROGRESS, Percentage of vectors parsed=100%-completed
WP-I-VECS, Total of 269 vectors read
WP-I-DELTA, Smallest delta =100.00 ps
WP-I-PIN, Read in the test patterns
W2TN-S-IN, Successfully loaded ELDO database
SECTION 18—check all pins (step S19)
W2TB-I-VERIFY, Verifying pin 'f1'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f2'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f3'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f4'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f5'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f6'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f7'
W2TB-I-STAT, This pin failed 1 times
WT2B-I-STAT, A total of 1 pins failed verification
WT2B-E-FAL, the HDL model is different to the ELDO response

It should be appreciated that embodiments of the present invention may be implemented by a computer program or by suitable circuitry. The various circuits described can be implemented in hardware or software. When the verification process has been completed an output signal is provided which indicates if the test has been successful or has failed.

The output of embodiments of the invention provides an indication to a user, for example, on a screen indicating that a test has failed or passed. Optionally, in the case of failure, an explanation as to the cause of failure is provided. The output may also advise the computer operating system if the test has passed and failed. In a preferred embodiment of the invention, a file is created in the operating system which indicates if a test has passed or failed. In the case of failure, the reasons for the failure are written in the file.

As an alternative to VHDL, Verilog can be used.

Embodiments of the present invention can be used to verify models of part or all of an integrated circuit.

It will be apparent to those skilled in the art that modifications could be made to the above-described examples without departing from the scope of the present invention.

What is claimed is:

1. A method of distinguishing between an input and output signal on a bi-directional pin of a model of a hardware circuit the steps of:

for a bi-directional pin of said signals to said bi-directional pin at a reduced drive strength such that

a driven signal on said bi-directional pin will be superimposed over the applied signal; and

measuring the drive strength of the signal on the bi-directional pin and responsive to said measurement determining whether the bi-directional pin is an input or output.

2. A method as claimed in claim 1, further comprising the step of providing an output to indicate if the bi-directional pin is an input or an output.

3. A method according to claim 1 wherein said model is a digital model.

4. A method according to claim 3 wherein said digital model is a HDL model.

5. A method as claimed in claim 4, wherein the HDL model utilizes the standard HDL values and a strong signal on the bi-directional pin is replaced by a Z in said applying step.

6. A method according to claim 1, wherein any output from said model has a drive strength greater than said reduced drive strength.

7. A computer program comprising program code that, when executed on a computer, perform any of the steps of any of claims 1 to 6.

8. A system for distinguishing between an input and output signal on a bi-directional pin of a model of a hardware circuit, said system comprising:

means for applying signals to a bi-directional pin of said model at a reduced drive strength such that a driven signal on said pin will be super imposed over the applied signal; and

means for measuring the drive strength of the signal on the bi-directional pin and responsive to said measurement determining whether the bi-directional pin is an input or output.

9. A system as claimed in claim 8, wherein said system is a computer system.

* * * * *

DETAILED ACTION

1. The following is a Notice of Allowability in response to Amendment received on 09 July 2004. Claims 1 and 7 have been amended. Claims 1-9 remain pending in this application.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Reg. No. on 09 September 2004.

The application has been amended as follows:

IN THE CLAIMS:

Claim 1, lines 3 and 4, deleted "said pin" and inserted "said bi-directional pin".

Claim 7, line 4, deleted "said pin" and inserted "said bi-directional pin".

IN THE CLAIMS

Please amend the claims as shown below.

1. (Currently Amended) A method of distinguishing between an input and [[or]] output signal on a bi-directional pin of a model of a hardware circuit, comprising the steps of:

for a bi-directional pin of said model, applying signals to said pin at a reduced drive strength such that a driven signal on said pin will be superimposed over the applied signal; and

measuring ~~comparing~~ the drive strength of the signal on the bi-directional pin and responsive to said measurement ~~comparison~~ determining whether the bi-directional pin is an input or output.

2. (Original) A method as claimed in claim 1, further comprising the step of providing an output to indicate if the bi-directional pin is an input or an output.

3. (Previously Presented) A method according to claim 1 wherein said model is a digital model.

4. (Original) A method according to claim 3 wherein said digital model is a HDL model.

5. (Previously Presented) A method as claimed in claim 4, wherein the HDL model utilizes the standard HDL values and a strong signal on the bi-directional pin is replaced by a Z in said applying step.

6. (Previously Presented) A method according to claim 1, wherein any output from said model has a drive strength greater than said reduced drive strength.

7. (Currently Amended) A system for distinguishing between an input [[or]] and output signal on a bi-directional pin of a model of a hardware circuit, said system comprising:

means for applying signals to a bi-directional pin of said model at a reduced drive strength such that a driven signal on said pin will be super imposed over the applied signal; and

means for ~~comparing~~ measuring the drive strength of the signal on the bi-directional pin and responsive to said measurement ~~comparison~~ determining whether the bi-directional pin is an input or output.

8. (Original) A system as claimed in claim 7, wherein said system is a computer system.

9. (Previously Presented) A computer program comprising program code that, when executed on a computer, perform any of the steps of any of claims 1 to 6.

PTO/SB/44 (04-04)
Approved for use through 04/30/2007
U.S. Patent and Trademark Office; US. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,926

DATED : January 25, 2005

INVENTOR(S) : Peter Ballam

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 18, line 65 should read:
--circuit comprising the steps of--

Col. 18, line 66 should read:
--for a bi-directional pin of said bi-directional signals to said --

Col. 20, line 10 should read:
--signal on said pin will be super imposed over the --

MAILING ADDRESS OF SENDER

PATENT NO. 6,847,926

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FEB 0 7 2005